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uATX(243.84mm X 203.2mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:Realtek RTM875N-632

HD Audio Codec:ALC887-VD-GR

LAN:RTL8111E 10/100/1000

IO: Fintek F71858AD

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PWM:

Controller:NCP5395 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *4

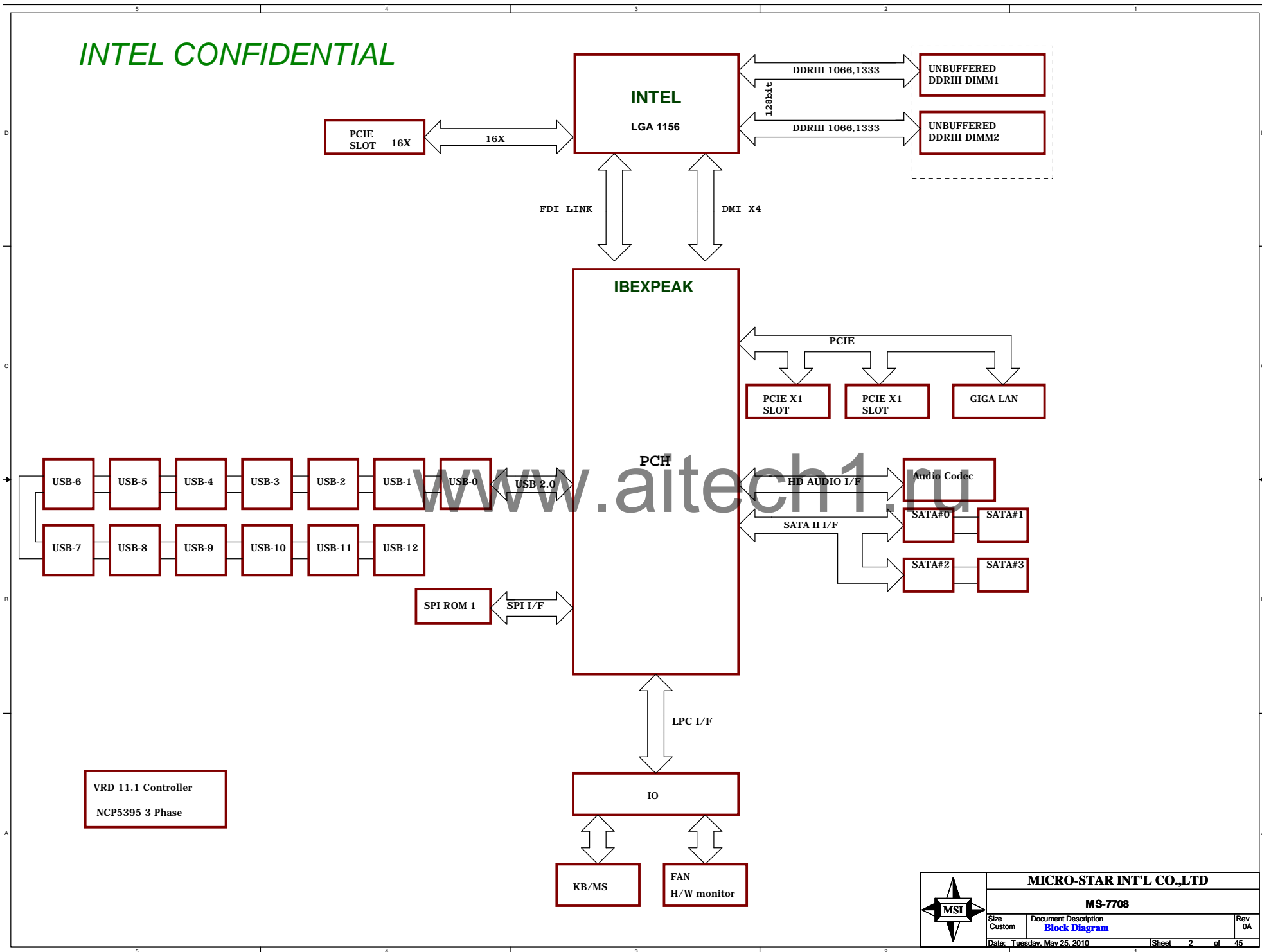
USB2.0 *10 (Rear*4 / Front*4)

USB3.0*2

On BOARD BUZZER

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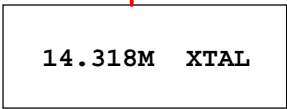
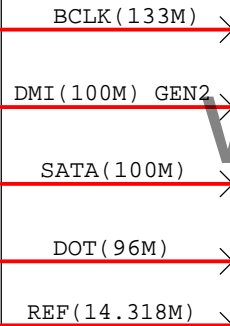
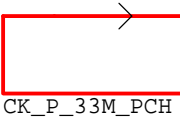
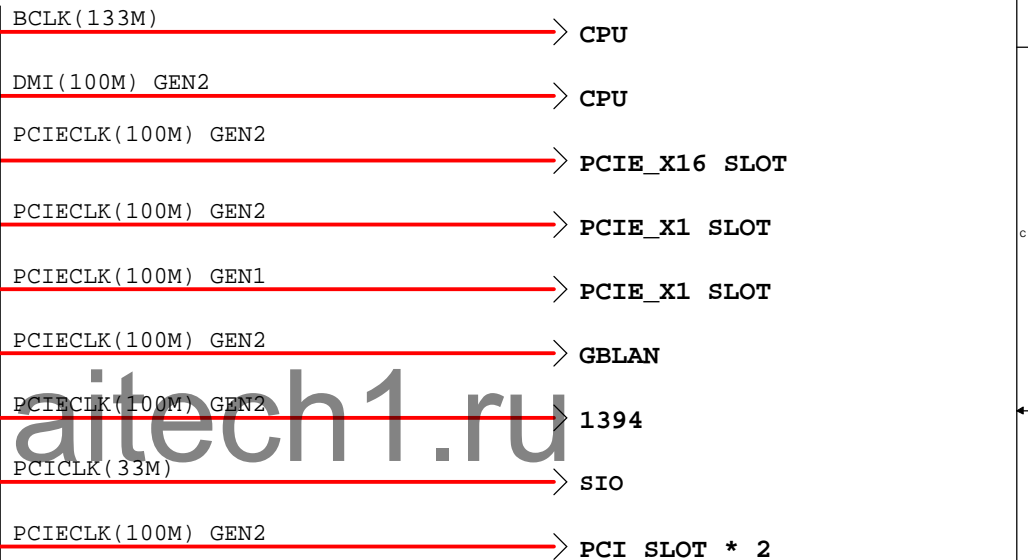
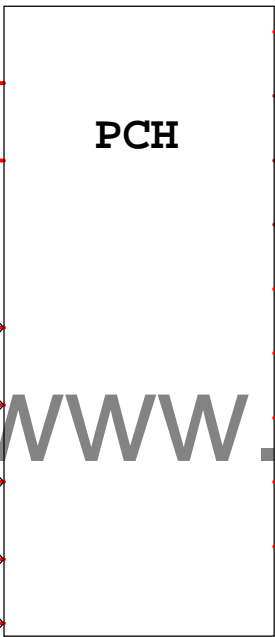
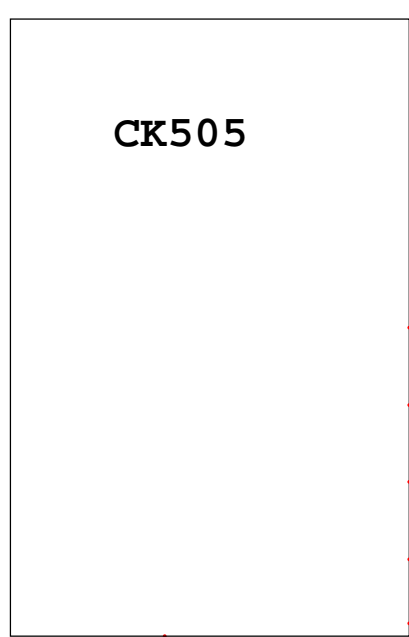
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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9.
USB PORT MAPPING **SUBJECT TO CHANGE**

Controller ^a	Port ^a	Destination ^a	Used ^b	ESD ^c Pads ^d	Bulk Cap ^e	Over-Current Detection ^f
JHC 4 Pin USB ^g	Port 1	Internal (Ready-To-Go) - F 50 ^h	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 2	Internal (Ready-To-Go) - F 51 ^h	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
JHC 4 Pin USB ^g	Port 3	Internal (Ready-To-Go) - F 52 ^h	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 4	Internal (Ready-To-Go) - F 53 ^h	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
JHC 4 Pin USB ^g	Port 5	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 6	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
JHC 4 Pin USB ^g	Port 7	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 8	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
JHC 4 Pin USB ^g	Port 9	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 10	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
JHC 4 Pin USB ^g	Port 11	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 12	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
JHC 4 Pin USB ^g	Port 13	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ
	Port 14	Front I/O ^j	Yes ⁱ	Yes ⁱ	Yes ⁱ	Yes ⁱ





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13 MEM_MA_DATA[63:0]

13 MEM_MA_ADD[15:0]

13 MEM_MA_WE_L
13 MEM_MA_CAS_L
13 MEM_MA_RAS_L

13 MEM_MA_BANK0
13 MEM_MA_BANK1
13 MEM_MA_BANK2

13 MEM_MA_CS_L0
13 MEM_MA_CS_L1
13 MEM_MA_CS_L2
13 MEM_MA_CS_L3

13 MEM_MA_CKE0
13 MEM_MA_CKE1
13 MEM_MA_CKE2
13 MEM_MA_CKE3

13 MEM_MA_ODT0
13 MEM_MA_ODT1
13 MEM_MA_ODT2
13 MEM_MA_ODT3

13 MEM_MA_CLK_H0
13 MEM_MA_CLK_L0
13 MEM_MA_CLK_H1
13 MEM_MA_CLK_L1
13 MEM_MA_CLK_H2
13 MEM_MA_CLK_L2
13 MEM_MA_CLK_H3
13 MEM_MA_CLK_L3

13 DDR3_DRAMRST#

CPU1A

SA_MA[0]
SA_MA[1]
SA_MA[2]
SA_MA[3]
SA_MA[4]
SA_MA[5]
SA_MA[6]
SA_MA[7]
SA_MA[8]
SA_MA[9]
SA_MA[10]
SA_MA[11]
SA_MA[12]
SA_MA[13]
SA_MA[14]
SA_MA[15]

SA_WE*
SA_CAS*
SA_RAS*
SA_BA[0]
SA_BA[1]
SA_BA[2]

SA_CS[0]*
SA_CS[1]*
SA_CS[2]*
SA_CS[3]*

SA_CKE[0]
SA_CKE[1]
SA_CKE[2]
SA_CKE[3]

SA_ODT[0]
SA_ODT[1]
SA_ODT[2]
SA_ODT[3]

SA_CK[0]
SA_CK[1]
SA_CK[1]*
SA_CK[2]
SA_CK[2]*
SA_CK[3]
SA_CK[3]*

SM_DRAMRST*

SA_CS[4]*
SA_CS[5]*
SA_CS[6]*
SA_CS[7]*

SA_DQS[8]
SA_DQS[8]*

SA_ECC_CB[0]
SA_ECC_CB[1]
SA_ECC_CB[2]
SA_ECC_CB[3]
SA_ECC_CB[4]
SA_ECC_CB[5]
SA_ECC_CB[6]
SA_ECC_CB[7]

DDR_A

1 OF 12

SA_DQS[0]
SA_DQS[0]*
SA_DM[0]

SA_DQ[0]
SA_DQ[1]
SA_DQ[2]
SA_DQ[3]
SA_DQ[4]
SA_DQ[5]
SA_DQ[6]
SA_DQ[7]

SA_DQS[1]
SA_DQS[1]*
SA_DM[1]

SA_DQ[8]
SA_DQ[9]
SA_DQ[10]
SA_DQ[11]
SA_DQ[12]
SA_DQ[13]
SA_DQ[14]
SA_DQ[15]

SA_DQS[2]
SA_DQS[2]*
SA_DM[2]

SA_DQ[16]
SA_DQ[17]
SA_DQ[18]
SA_DQ[19]
SA_DQ[20]
SA_DQ[21]
SA_DQ[22]
SA_DQ[23]

SA_DQS[3]
SA_DQS[3]*
SA_DM[3]

SA_DQ[24]
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SA_DM[4]

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SA_DQ[63]

AK3
AJ3
AJ2

AH1
AL2
AL1
AG2
AH2
AK1
AK2

AP2
AP3
AN1

AN3
AN2
AR3
AR2
AM3
AM2
AP1
AR4

AJ4
AJ3
AJ1

AT4
AU2
AW3
AW4
AT3
AT1
AV2
AV4

AJ6
AW6
AV6

AW5
AY5
AU8
AY8
AU5
AV7
AW7

AR28
AT28
AV29

AN27
AT28
AP28
AP30
AN26
AR27
AR29
AN30

AV32
AW32
AW31

AJ30
AJ31
AJ33
AJ34
AJ30
AW30
AJ33
AW33

AW36
AV35
AJ35

AW35
AY35
AV37
AJ37
AY34
AW34
AJ36
AW37

AR39
AR38
AT38

AT39
AT40
AN38
AN38
AJ38
AP39
AP40

MEM_MA_DQS_H0 13
MEM_MA_DQS_L0 13
MEM_MA_DM0 13

MEM_MA_DATA0
MEM_MA_DATA1
MEM_MA_DATA2
MEM_MA_DATA3
MEM_MA_DATA4
MEM_MA_DATA5
MEM_MA_DATA6
MEM_MA_DATA7

MEM_MA_DQS_H1 13
MEM_MA_DQS_L1 13
MEM_MA_DM1 13

MEM_MA_DATA8
MEM_MA_DATA9
MEM_MA_DATA10
MEM_MA_DATA11
MEM_MA_DATA12
MEM_MA_DATA13
MEM_MA_DATA14
MEM_MA_DATA15

MEM_MA_DQS_H2 13
MEM_MA_DQS_L2 13
MEM_MA_DM2 13

MEM_MA_DATA16
MEM_MA_DATA17
MEM_MA_DATA18
MEM_MA_DATA19
MEM_MA_DATA20
MEM_MA_DATA21
MEM_MA_DATA22
MEM_MA_DATA23

MEM_MA_DQS_H3 13
MEM_MA_DQS_L3 13
MEM_MA_DM3 13

MEM_MA_DATA24
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MEM_MA_DATA26
MEM_MA_DATA27
MEM_MA_DATA28
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MEM_MA_DATA30
MEM_MA_DATA31

MEM_MA_DQS_H4 13
MEM_MA_DQS_L4 13
MEM_MA_DM4 13

MEM_MA_DATA32
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MEM_MA_DATA37
MEM_MA_DATA38
MEM_MA_DATA39

MEM_MA_DQS_H5 13
MEM_MA_DQS_L5 13
MEM_MA_DM5 13

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MEM_MA_DATA45
MEM_MA_DATA46
MEM_MA_DATA47

MEM_MA_DQS_H6 13
MEM_MA_DQS_L6 13
MEM_MA_DM6 13

MEM_MA_DATA48
MEM_MA_DATA49
MEM_MA_DATA50
MEM_MA_DATA51
MEM_MA_DATA52
MEM_MA_DATA53
MEM_MA_DATA54
MEM_MA_DATA55

MEM_MA_DQS_H7 13
MEM_MA_DQS_L7 13
MEM_MA_DM7 13

MEM_MA_DATA56
MEM_MA_DATA57
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MEM_MA_DATA60
MEM_MA_DATA61
MEM_MA_DATA62
MEM_MA_DATA63

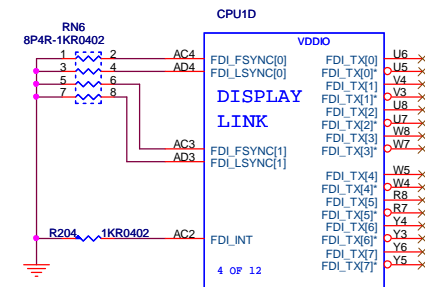
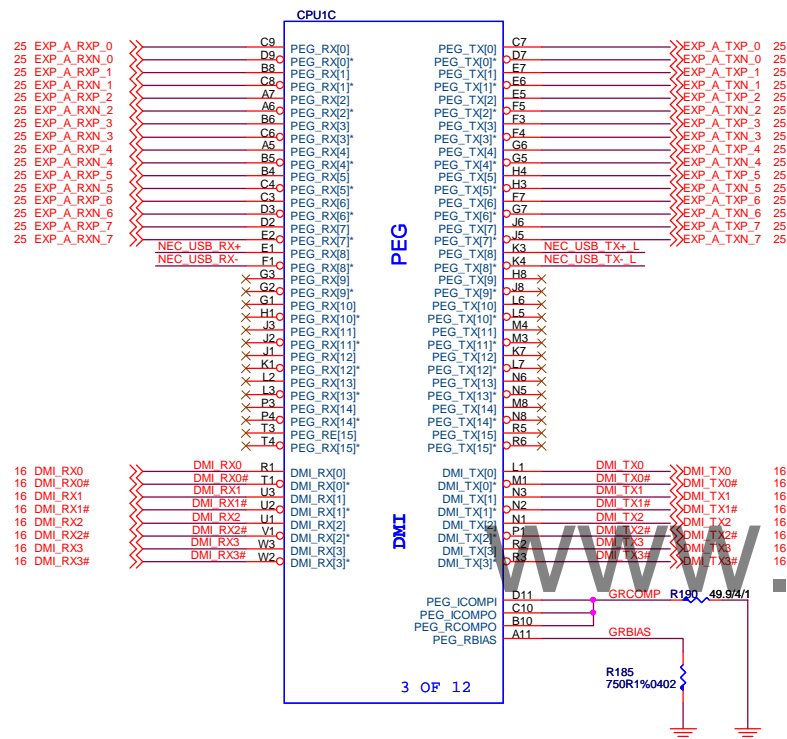
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24.24 Intel® Flexible Display Interface (Intel® FDI)

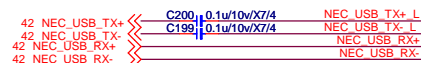
Table 24-36. Intel® Flexible Display Interface Signals

Signal	Type	Recommendation	Resistor/Impedance
FDI_RXP[7:0]	I	Connect to VDDIO if not used.	
FDI_RXN[7:0]	I	Connect to VDDIO if not used.	
FDI_PVDD[1:0]	D	Connect to VDDIO if not used.	
FDI_TXP[7:0]	O	Connect to VDDIO if not used.	
FDI_TXN[7:0]	O	Connect to VDDIO if not used.	

433423_436423_Bromelow_Server_PDG_Rev.07.pdf

Table 7-6. Haverdale/Lynnfield PCI Express® and DMI Compensation Routing Guidelines

Signal Name	Width [W] / Spacing [S]	Length	Resistor	Notes
PEG_ICOMPO PEG_ICOMPI PEG_RCOMP PEG_RCOMPI	W = 10 mils S = 6 mils spacing for 300 mils at breakout, 15 mils spacing after that	0.4" ± 0.1"	48.9 Ω ± 1%	1
PEG_RBIAS	W = 10 mils S = 6 mils spacing for 300 mils at breakout, 15 mils spacing after that	0.4" ± 0.1"	750 Ω ± 1%	1

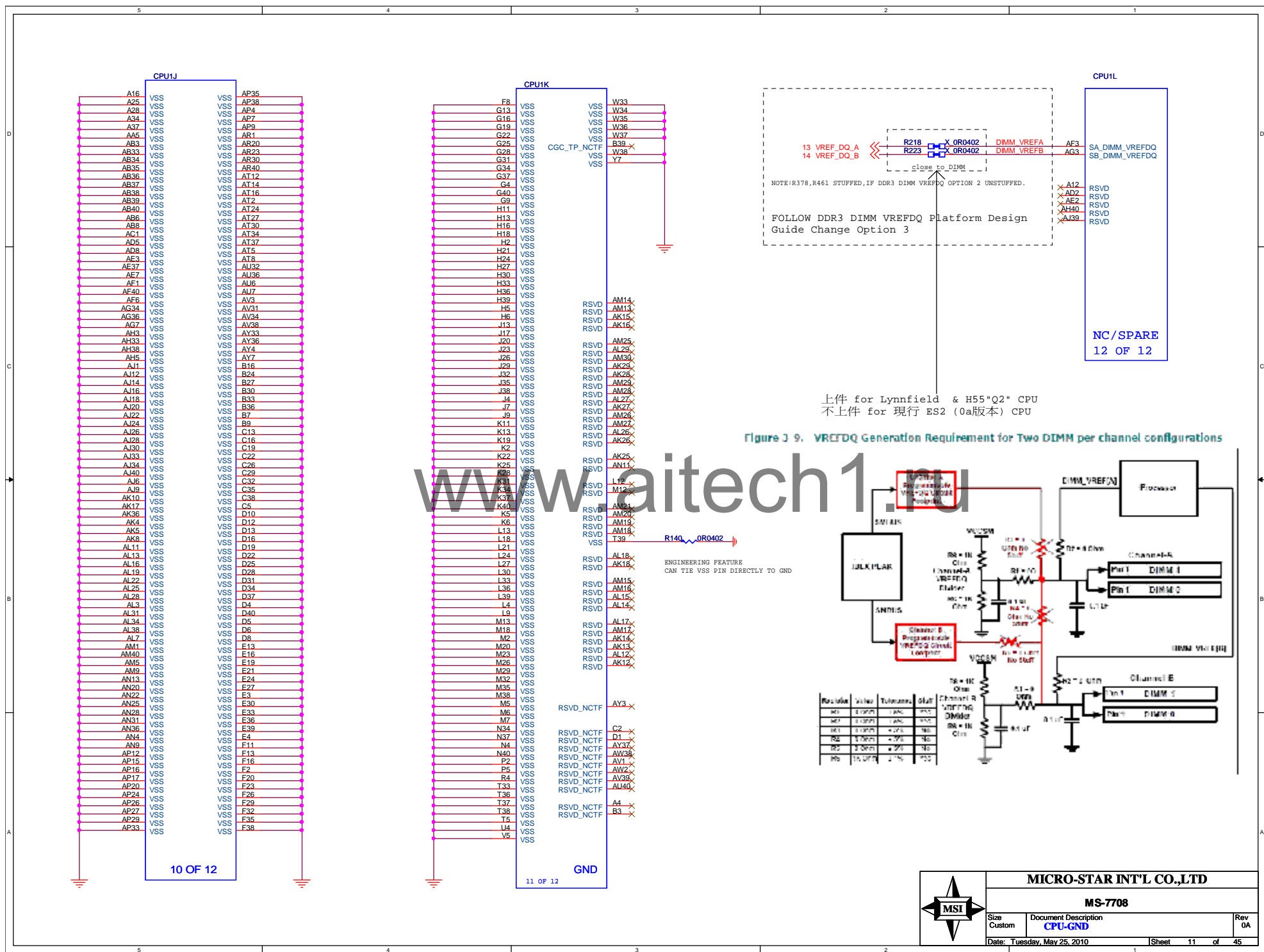


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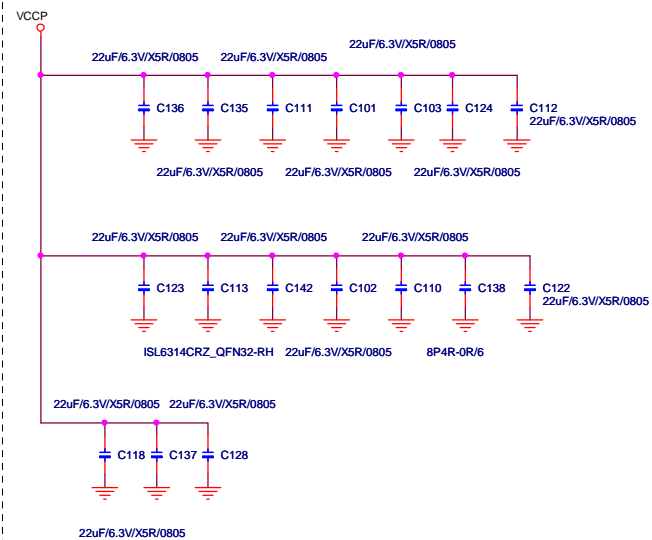
MS-7708

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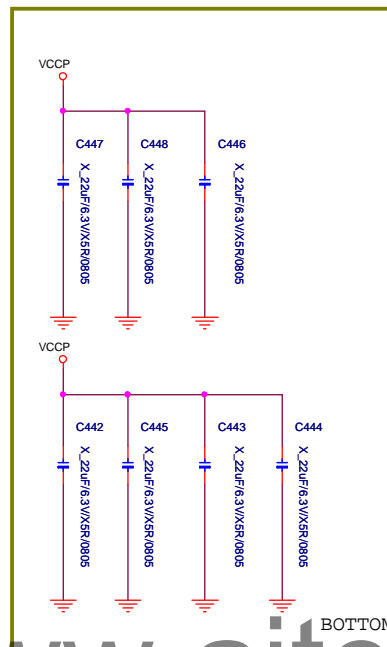




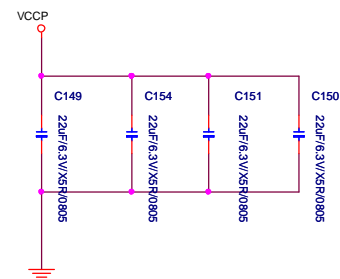
+CPU_VCCP-Decoupling



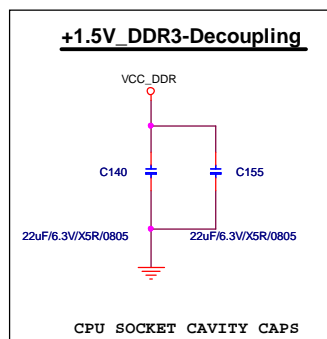
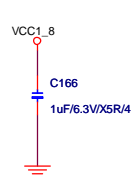
PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY



BOTTOM

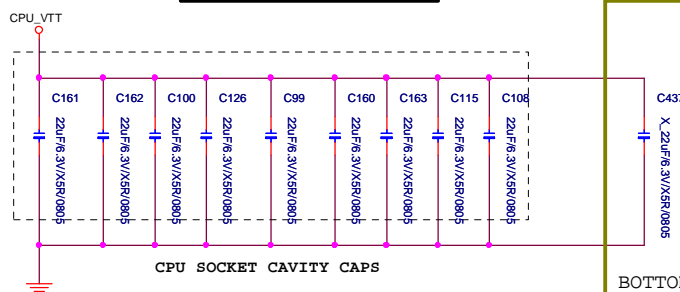


+1.5V_DDR3-Decoupling



CPU SOCKET CAVITY CAPS

+CPU_VTT Decoupling



CPU SOCKET CAVITY CAPS

BOTTOM

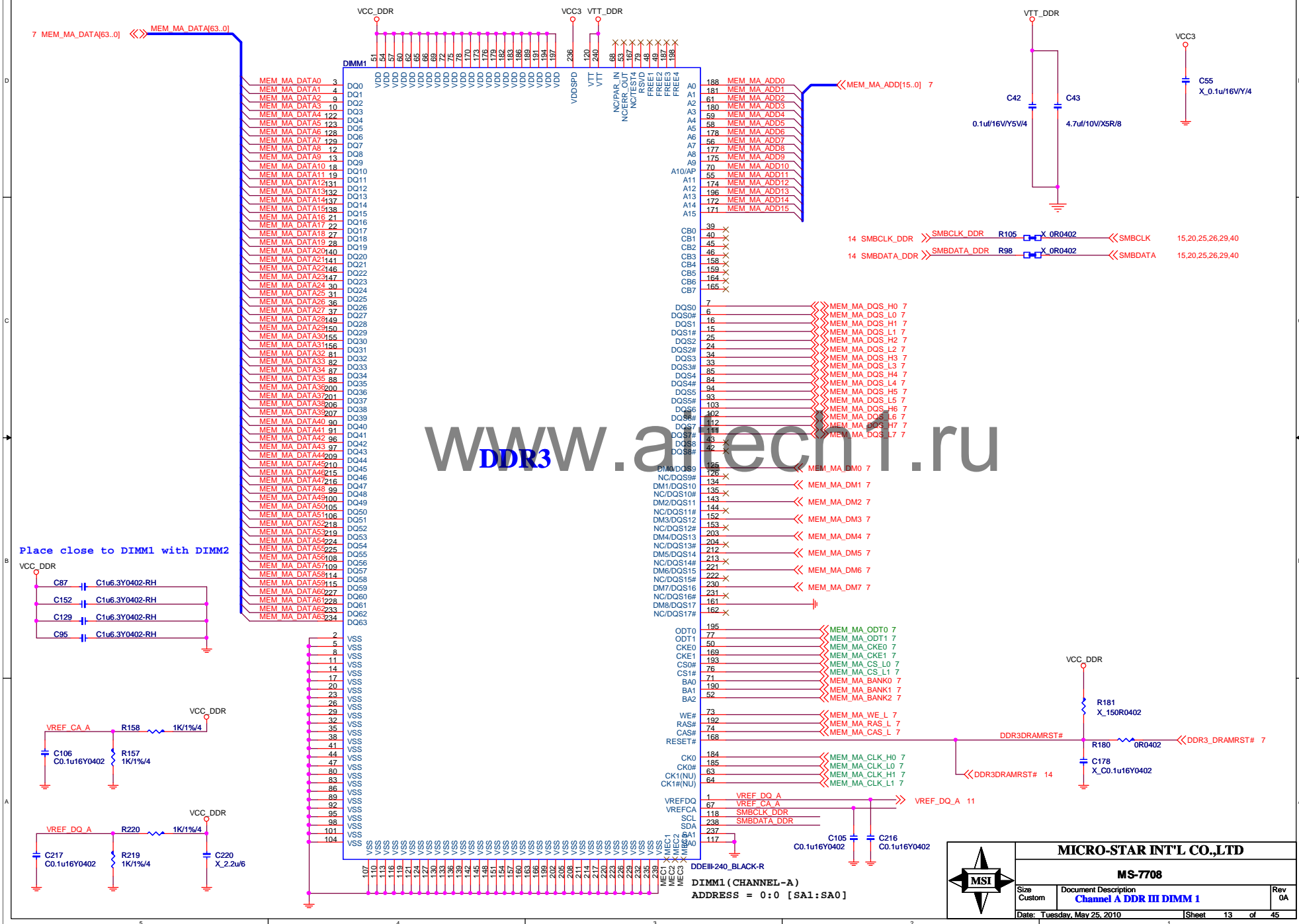


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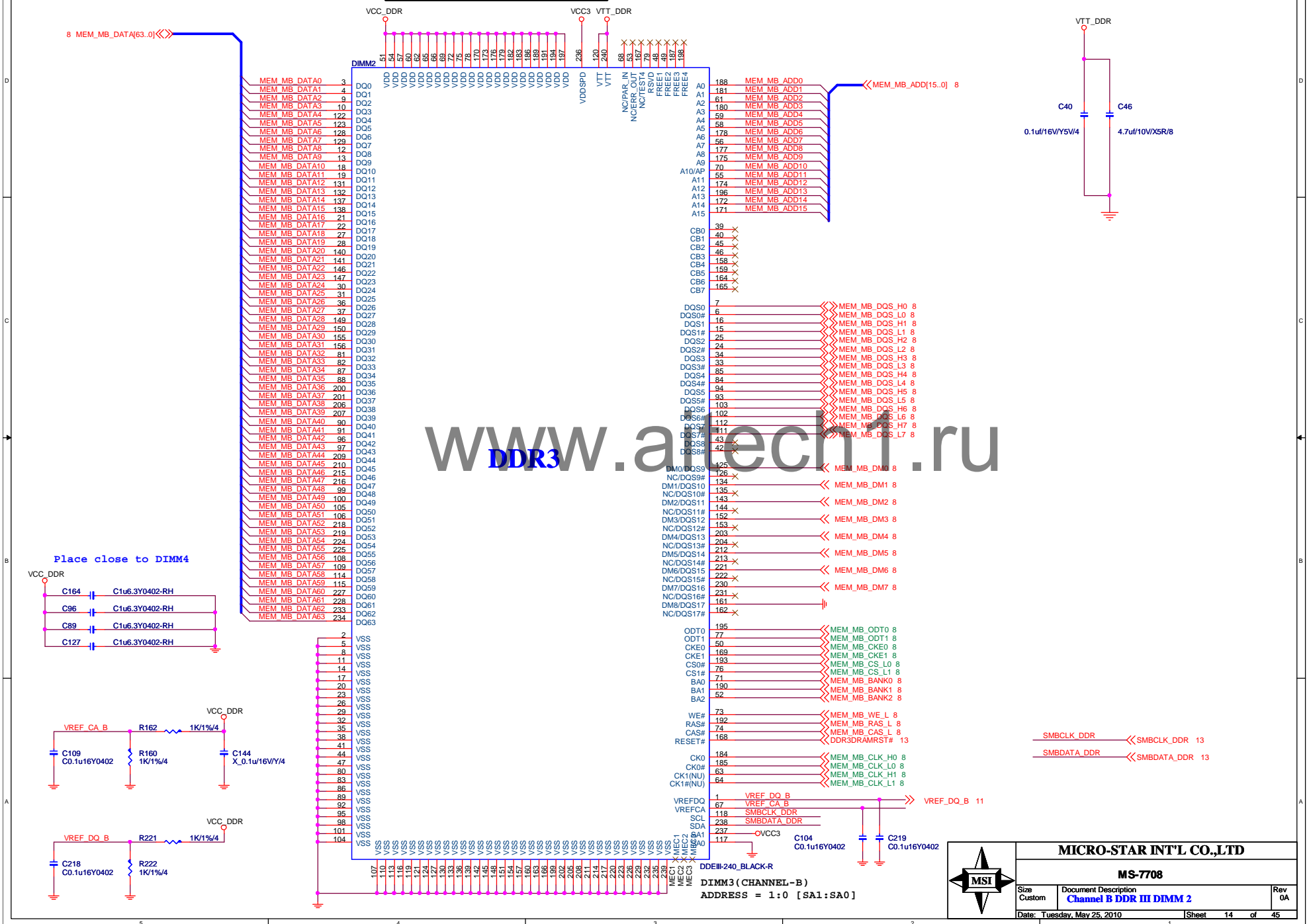
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		CPU-Decoupling	0A
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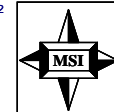
DDRIII DIMM_A1



DDRIII DIMM_B1



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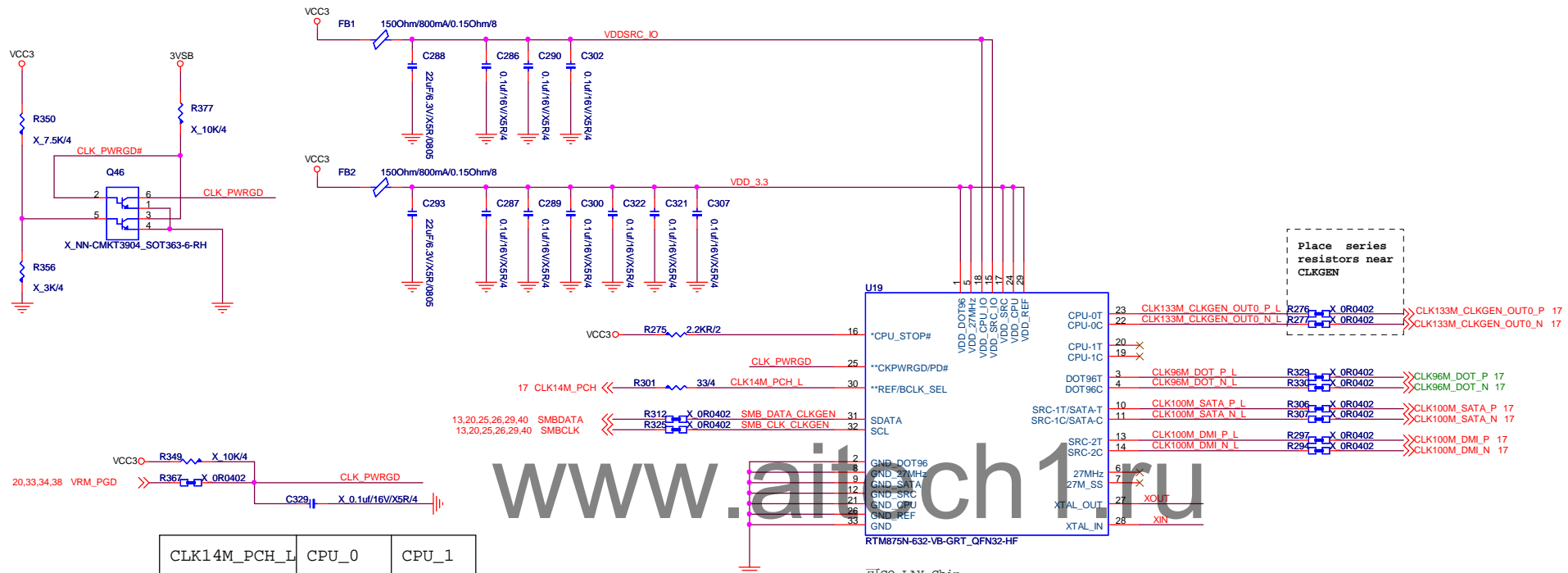


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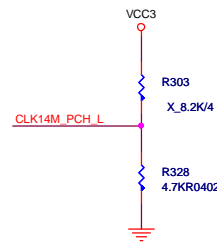
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CLOCK Gen / RTM875N-632



CLK14M_PCH_L	CPU_0	CPU_1
0	133	133
1 (0.7~1.5V)	100	100



CLOCK EMI CAPS: DEFAULT EMPTY

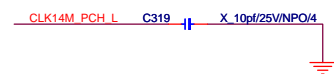
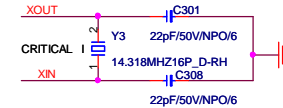
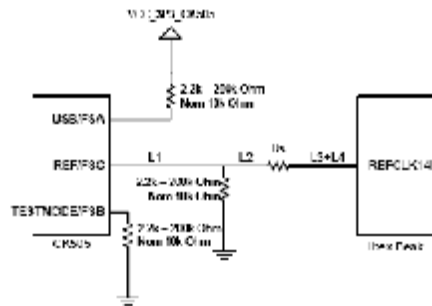


Figure 11-16. REFCLK Topology from CLKIN to the Peak with BCL EMI Frequency Shaping



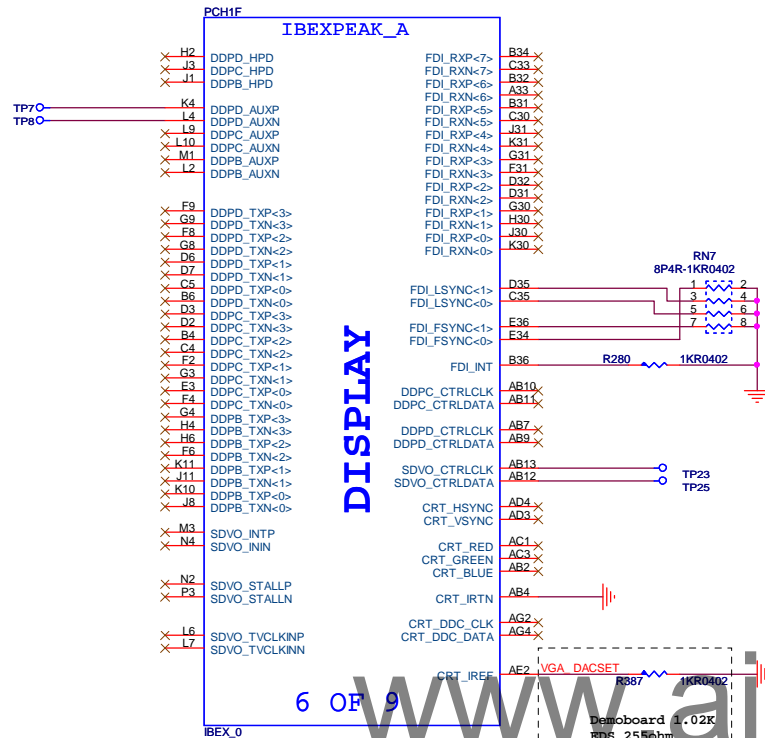
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Low under 0.8V
High over 2V



7.1.3.1 FDI Disable Guidelines

Following table describes recommendations for disabling FDI on the CPU.

FDI Signal	Recommendation
FDI_TX[7:0]	Float
FDI_LX# [7:0]	Float
FDI_FSYN<	Lk resistor to vcc_fdi or vss
FDI_LSYN<	Lk resistor to vcc_fdi or vss
FDI_INT	Lk resistor to vcc_fdi or vss

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1_5.pdf

Analog Display Recommendations - 376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1_5.pdf

Table 6-2. Analog Display Recommendations for Discrete Only Configurations

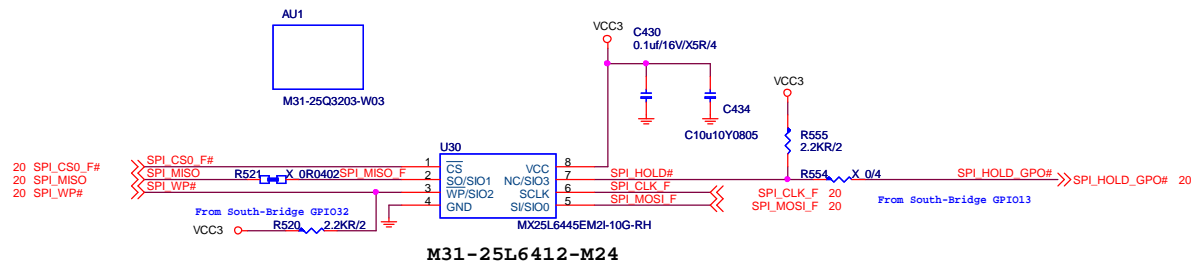
Signal Name	Recommended Connection
CRT_RED, CRT_GREEN, CRT_BLUE	NC or GND
CRT_IRRTN	GND
CRT_LSYN<, CRT_FSYN<	NC
DAC_TRFF	GND through 10k \pm 1%, 1%, or 0.5% resistor
DDPC_CLK, DDC_DATA	NC

For external graphics designs, the pins VccADPLLA, VccADPLLD, VccFDIPLL and VccADAC should be directly shorted to the respective power rails and no LC filters are required to be populated on the power rails that source these pins.

376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1_5.pdf

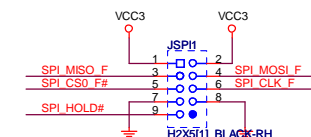
R492 from 1.02k to 0ohm if D-SUB Unuse.

SPI FLASH ROM



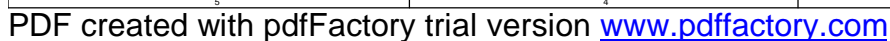
SPI DEBUG PROT

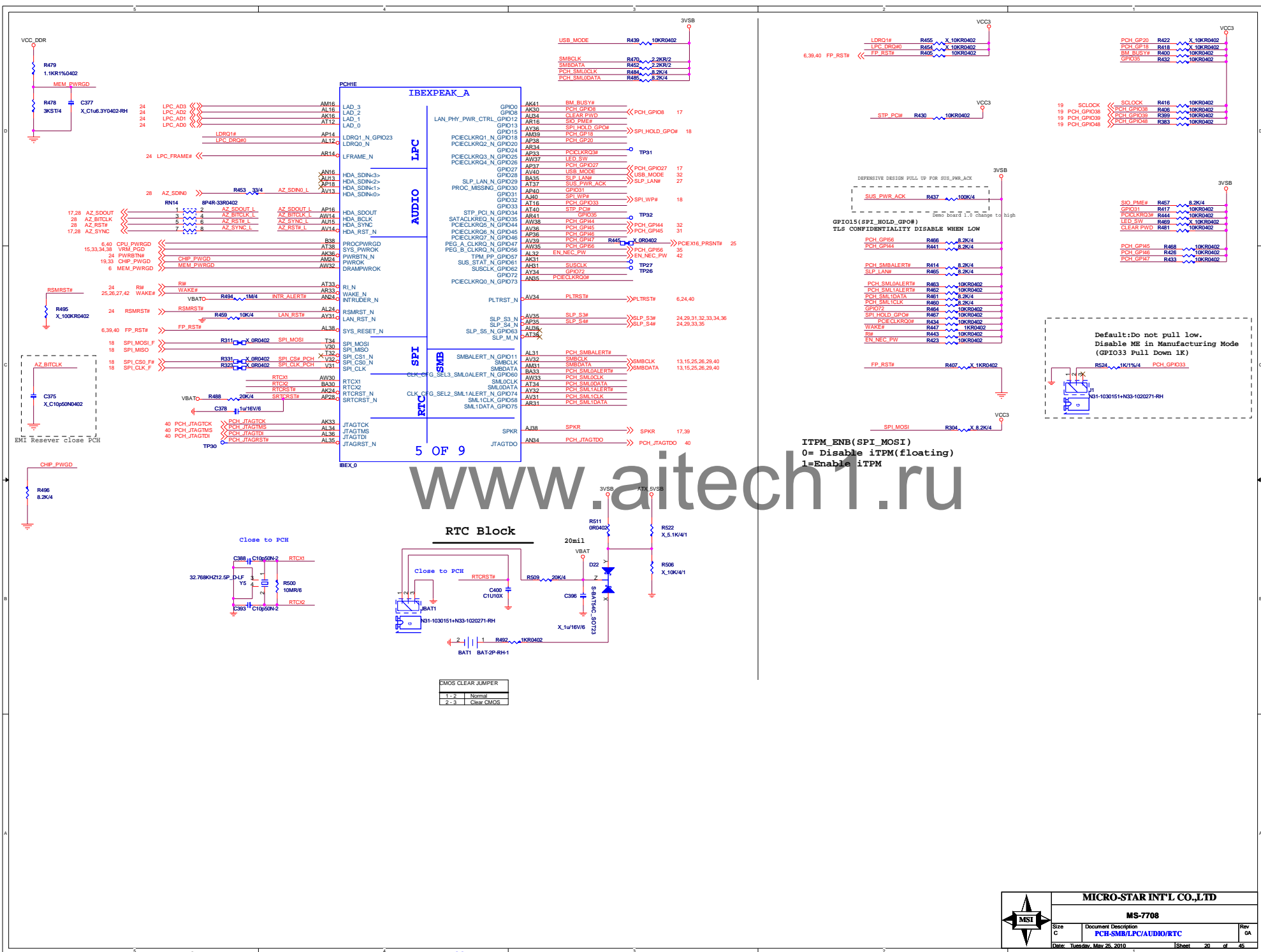
Close to SPI ROM



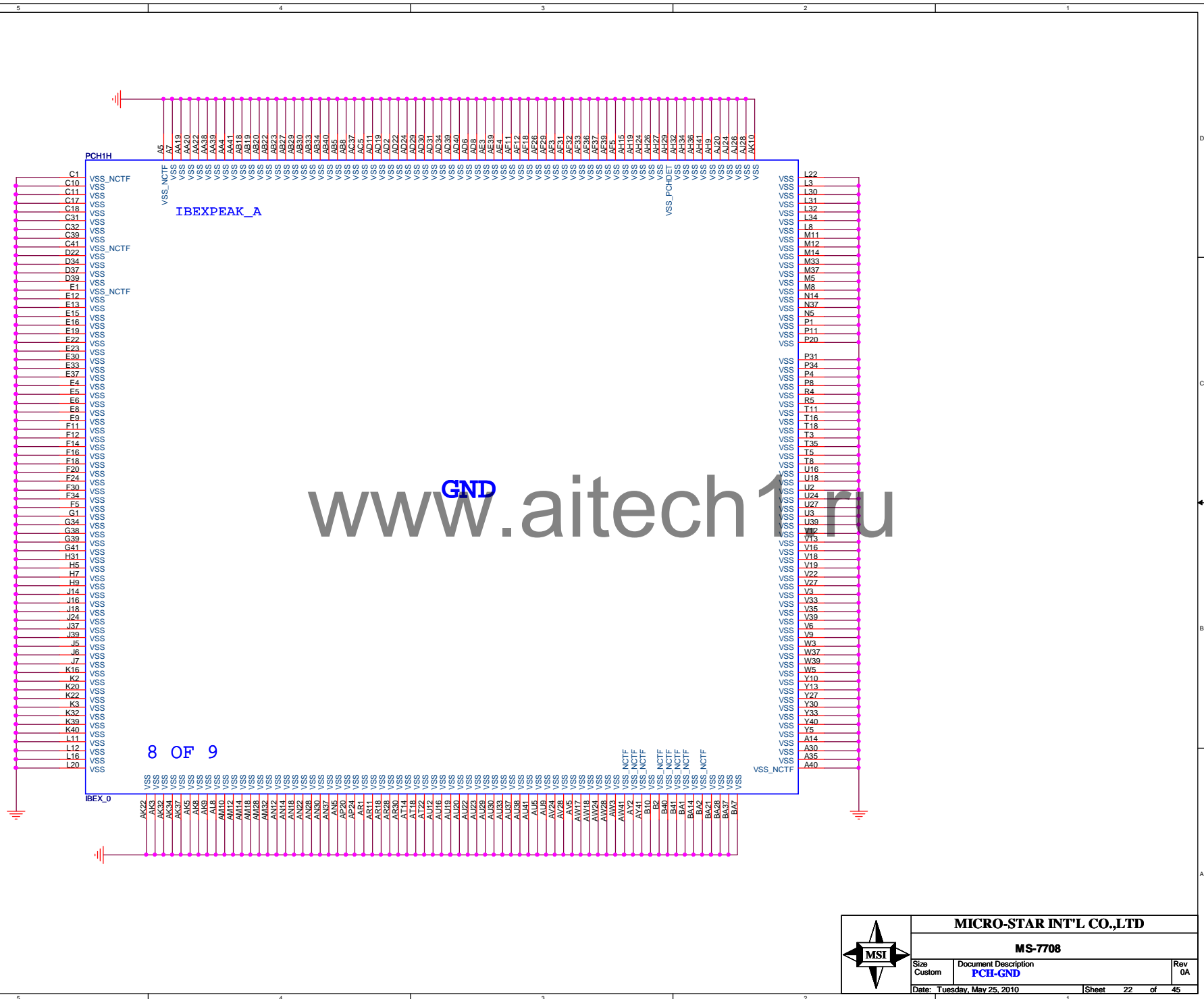
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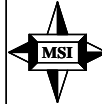
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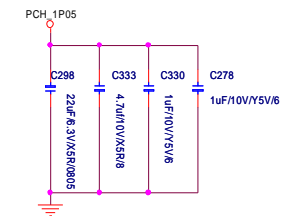
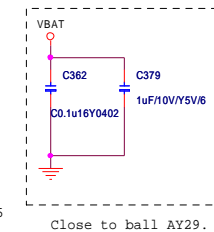
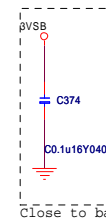
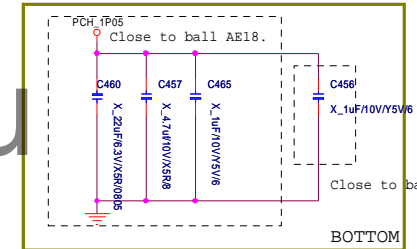
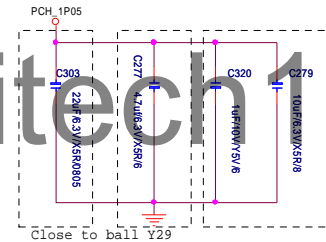
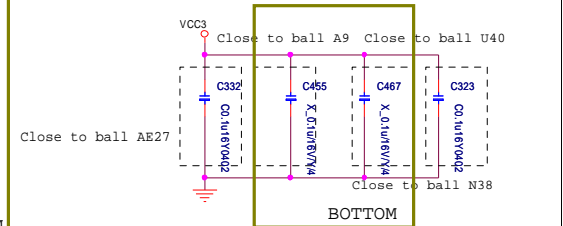
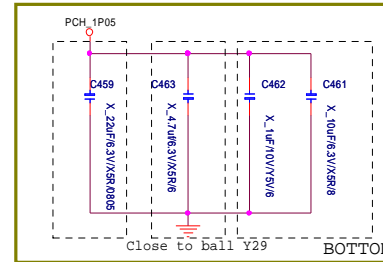
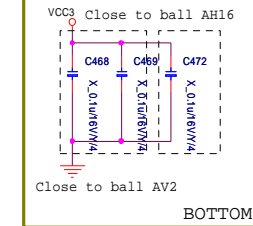
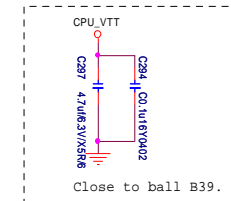
			MICRO-STAR INT'L CO.,LTD	
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		PCH-GND		
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PCH decoupling cap

Table 6-2. Analog Display Recommendations for Discrete Only Configurations

Signal Name	Recommended Connection
DET_RDET, DET_GREEN, DET_BLUE	NC or GND
CLK_IN_R	NC
CLK_SYNC, CLK_SYNC	NC
CLK_IN_U	GND through 1K0/10V, 1.5V, or 0.5V/5V/6V
DET_CLK, DET_DATA	NC

For external graphics designs, the pins VccADP1A, VccADP1B, VccFDIPLL and VccDAC should be directly connected to the respective power rails and no LC filters are required to be populated on the power rails that source these pins.



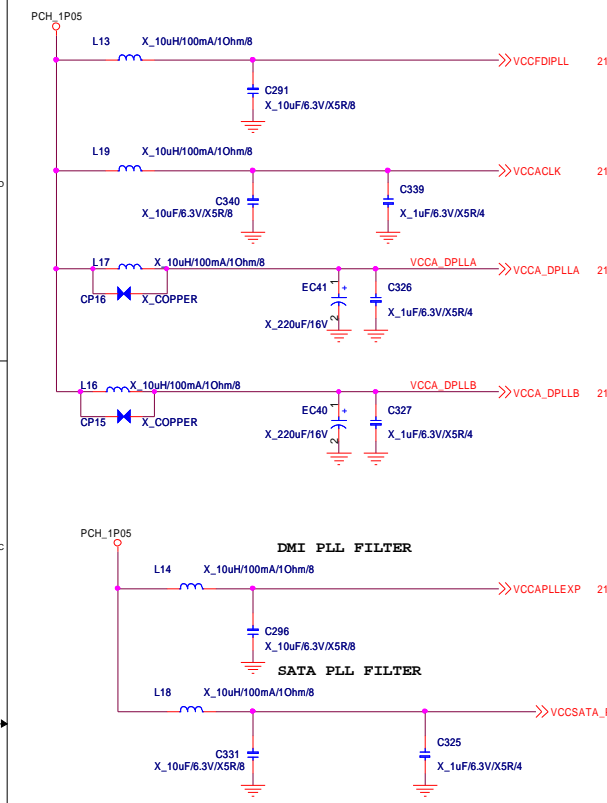
Signal	Correct Recommendation	Current Recommendation in design guide Rev 1.2
DAC_IRRT	1K0hm with +/- 5% (max 0.5%)	GND
VccADAC	V_1P05_PCH	Directly short the signal to 3.3V rail. No filters required



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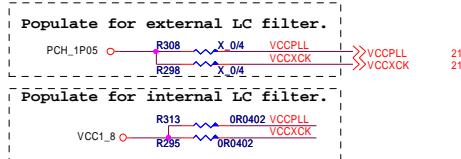
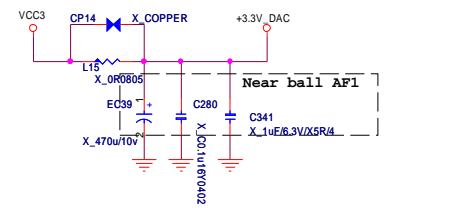
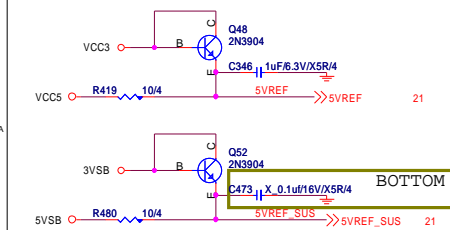
376563_376563_Piketon_Kings_Creek_Foxhollow_Platform_Design_Guide_Rev1_5.pdf

32.4.2 Internal VccVRM option:

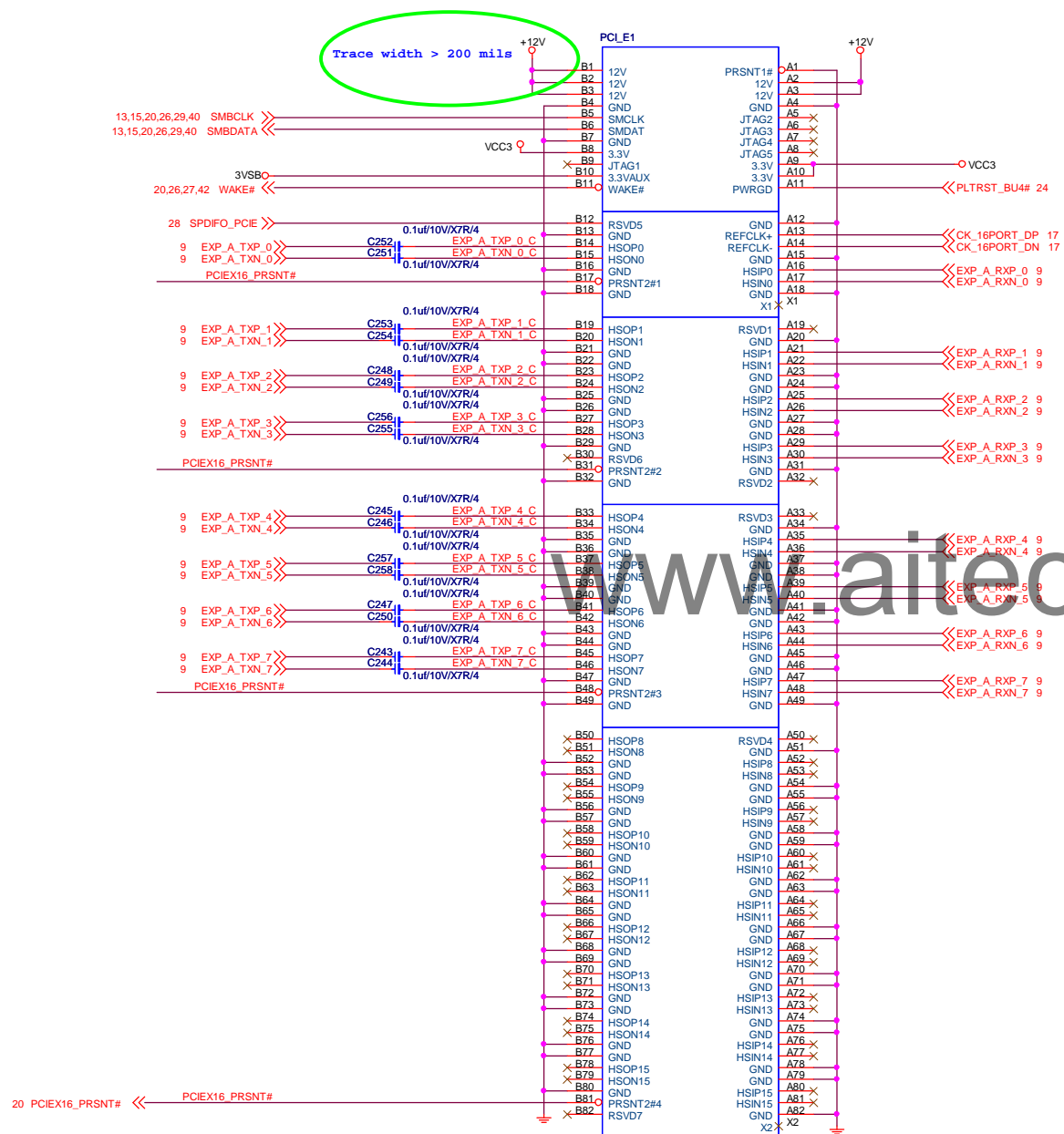
**The VccVRM rail (1.8V/1.5V) powers an internal voltage regulator module (VRM) that regulates clean 1.05V voltage supply for analog rails (VccAClk, VccaplleXP, VccFDIPLL, and VccSATAPLL). **This solution will allow us to remove the LC filter requirements for those rails, thereby reducing platform BOM cost. **To enable the internal VRM, VccVRM needs to be connected to 1.8V/1.5V, GPIO27 needs to be pulled high (customers can leave GPIO27 floating as there is an internal pull-up on pin), and VccAClk, VccaplleXP, VccFDIPLL, & VccSATAPLL should be left floating. HDA_SYNC signal is used as a strap to select whether VccVRM is connected to 1.8V or 1.5V. Refer to latest Intel R 5 Series Chipset EDS for more details.

5VREF & 5VREF_SUS Sequencing Circuit

V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



PCI_Express X16 Slot



SLOT-PC164P_BLACK-2PITCH-RH-16
N11-1640221-L06

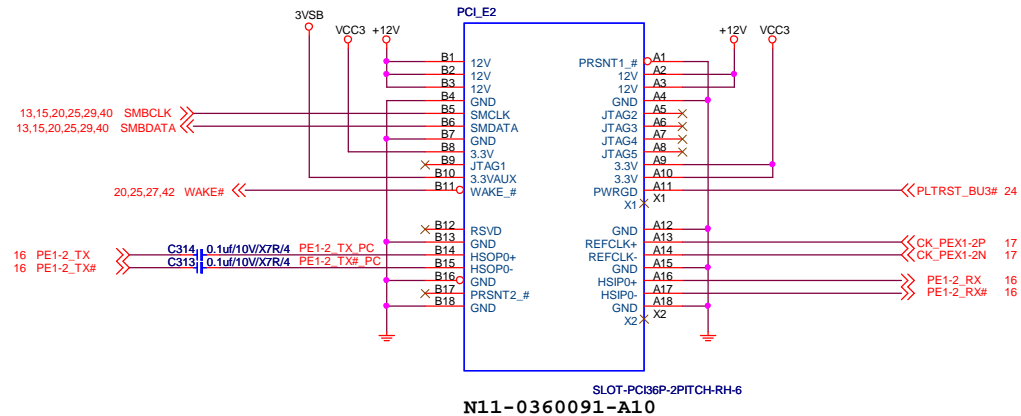


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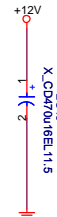
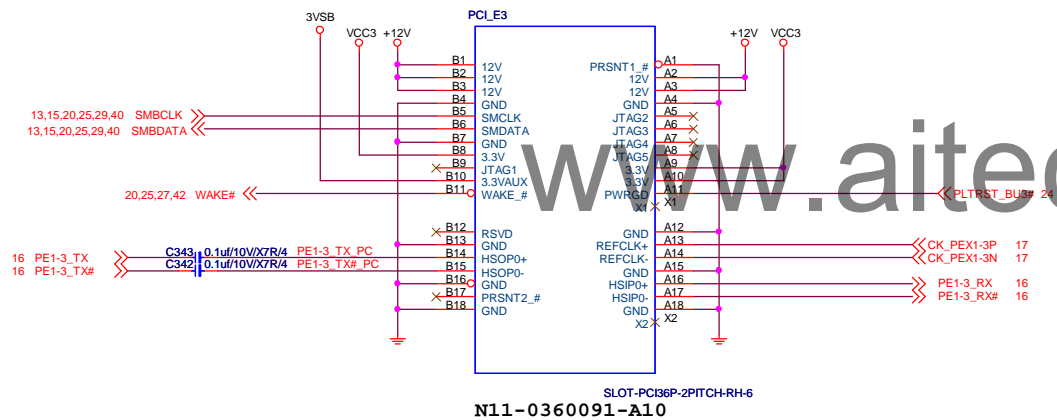
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PCI EXPRESS x1-PORT1



PCI EXPRESS x1-PORT2



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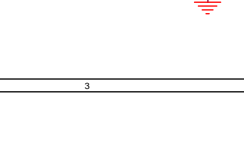
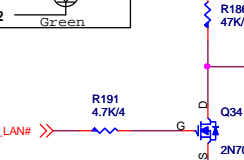
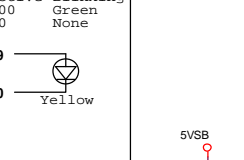
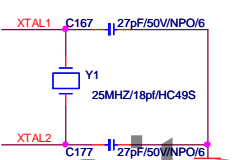
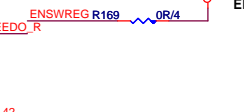
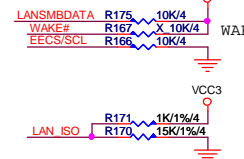
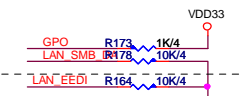
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Controller

R15 value should be 2.49K (1%) for all application.

Function (Efues)



WAKE# PCH端Pull High

C452 NEAR 3VDAUL

CH0KE2close to U9 Pin 36 within 0.5cm

CLOSE TO POWER PIN

CH0KE7

CH-4.7u.77A130mS-RH

CH0KE2

CH0KE7

CH0KE7

CH0KE7

CH0KE7

CH0KE7

CH0KE7

CH0KE7

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CH0KE7

CH0KE7

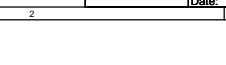
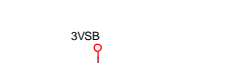
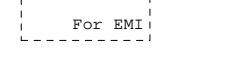
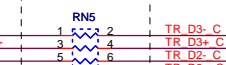
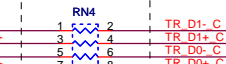
CH0KE7

CH0KE7

CH0KE7

CH0KE7

CH0KE7



Power consumption		
	1G	100M
3.3V	103mA	TBD
1.5V	367mA	TBD
1.8V	198mA	TBD

N58-16F0031-F02

Giga-Lan		10/100-Lan	
N58-22F0181-U30		N58-22F0061-S42 N58-22F0061-F02	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	1000	Orange
100	Green	100	Green
10	None	10	None
19	Yellow	19	Yellow
20	Yellow	20	Yellow
21	Orange	21	Orange
22	Green	22	Green

PMOS

Q32 P-P06P03LCG_SOT89-3-RH

3VSB_LAN

3VSB_LAN

3VSB_LAN

3VSB_LAN

3VSB_LAN

3VSB_LAN



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For 892&887-VD上件
For 662不上

5VSB

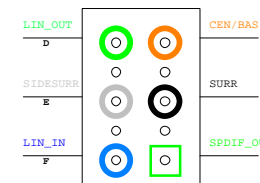
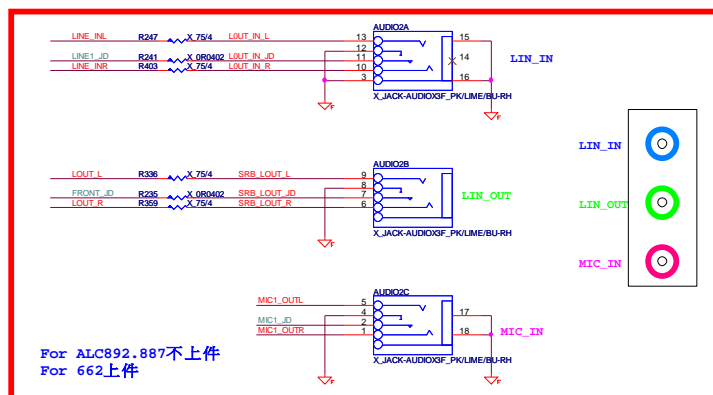
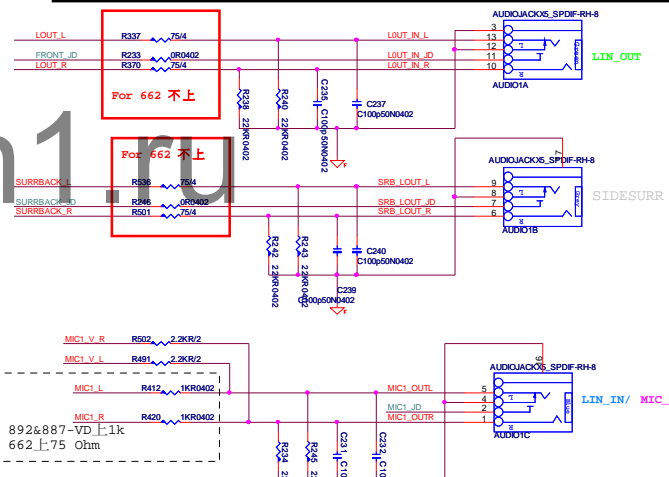
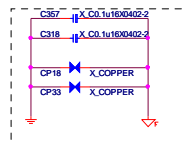
L30
180L230mA-300-RH


C386
0.1μF

C389
3.3kΩ

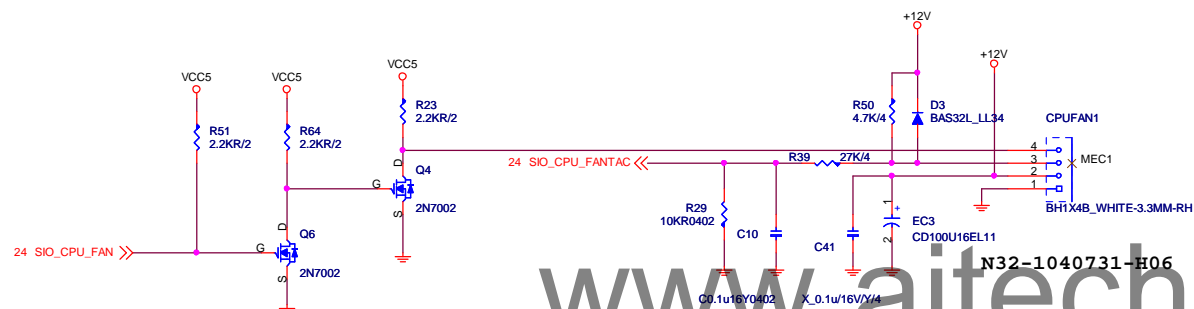
C106, 3X


LINE V R



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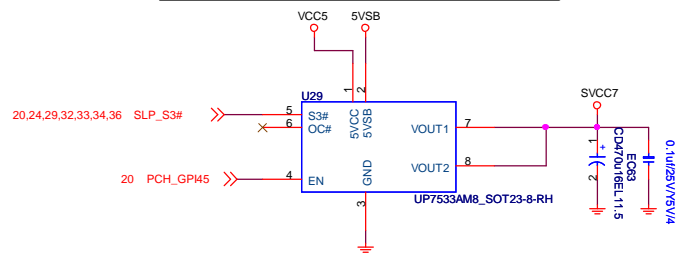
FAN-COUNTROL CIRCUIT



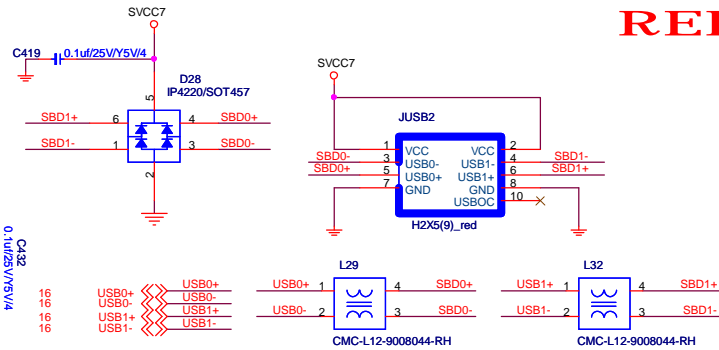
		MICRO-STAR INT'L CO.,LTD	
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FRONT POWER CONTROL

POWER CIRCUIT FOR USB PORT 0, 1

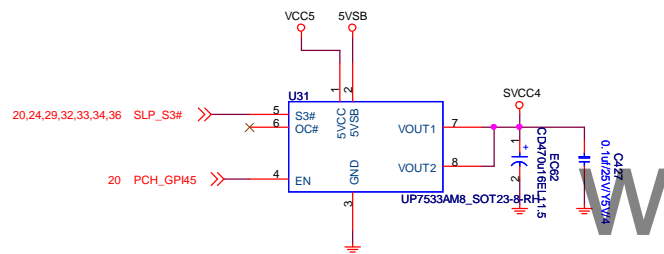


FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

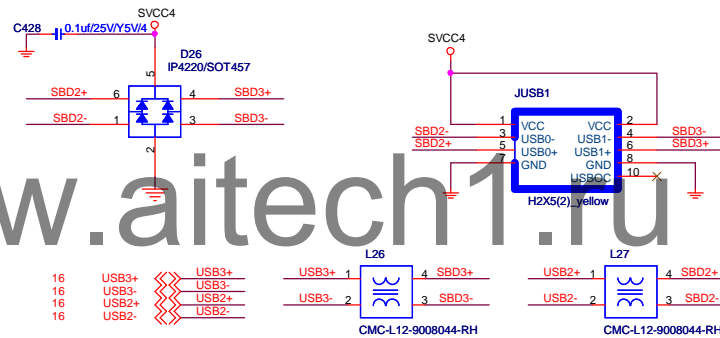


NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 2, 3

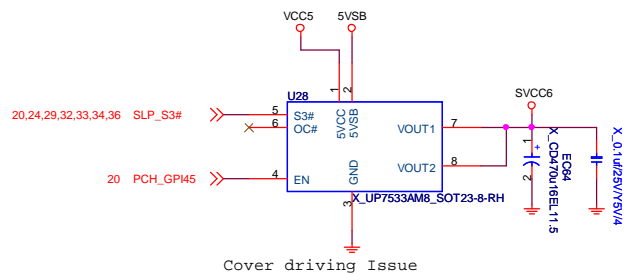


FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



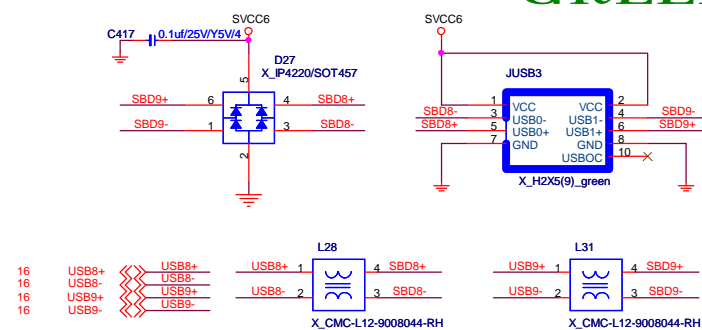
NEAR USB CONNECTOR

POWER CIRCUIT FOR USB PORT 8, 9



Cover driving Issue

FRONT PANEL USB CONNECTOR FOR USB PORT 8, 9



NEAR USB CONNECTOR

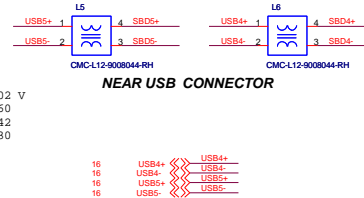
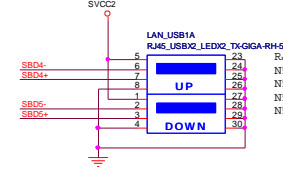
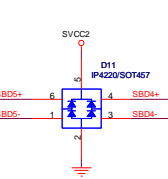


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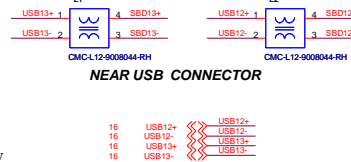
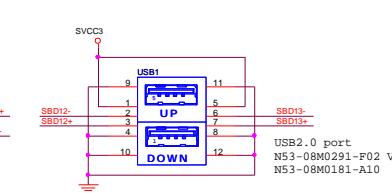
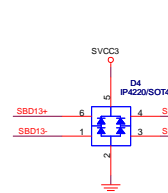
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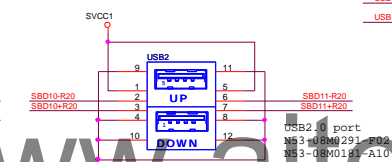
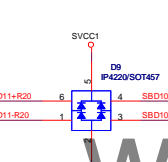
REAR PANEL USB/LAN CONNECTOR FOR USB PORT 4,5



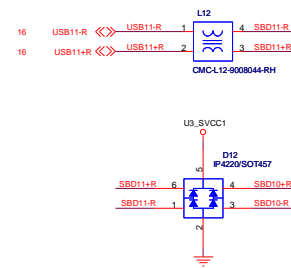
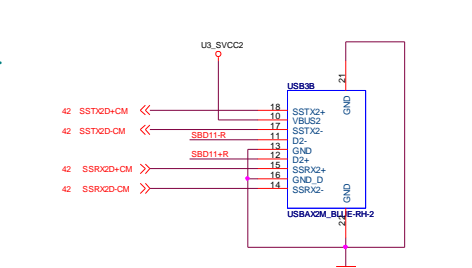
NEAR USB CONNECTOR



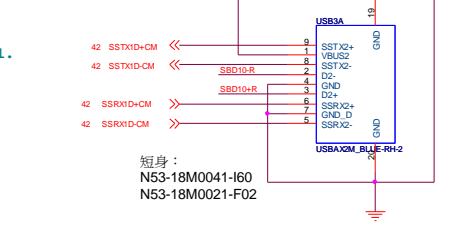
NEAR USB CONNECTOR

**NEAR REAR USB CONNECTOR**

Stuff for USB2.0



Connector	Power	GPIO Control
REAR USB Support S5 Power (KB/PS2/LAN)	SVCC1,SVCC2,SVCC3	USB_MODE
FRONT USB (JUSB1,JUSB2,JUSB3,JUSB4)	SVCC4,SVCC5,SVCC7	PCH_GPI45
USB3.0 Support S5 Power	U3_SVCC1,U3_SVCC2	PCH_GPI44



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Size

Document Description

Custom

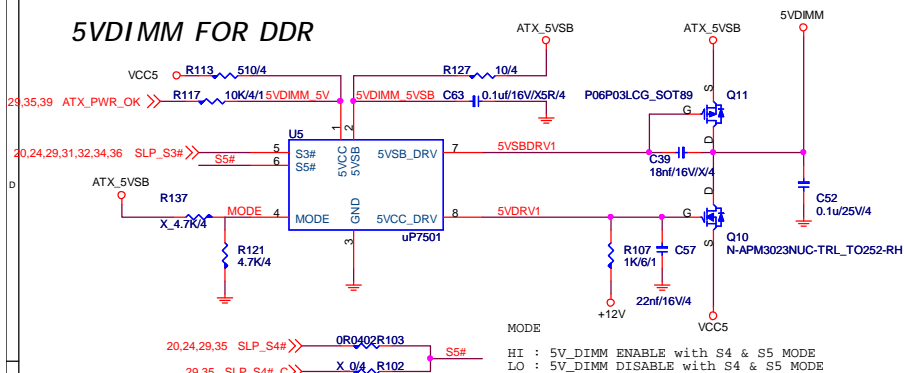
REAR USB&3.0

Date:

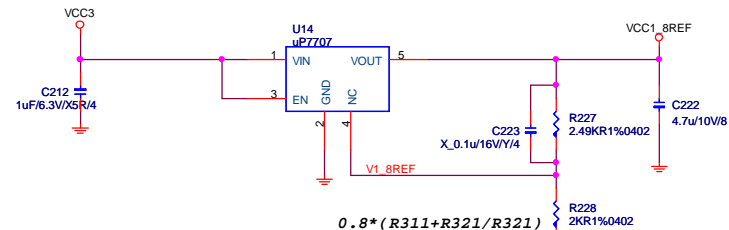
Tuesday, May 25, 2010

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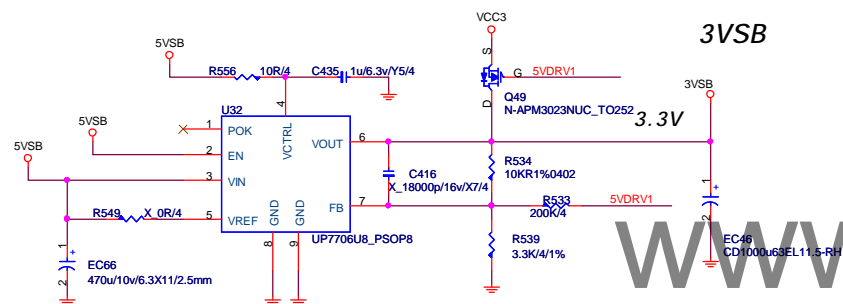
5VDIMM FOR DDR



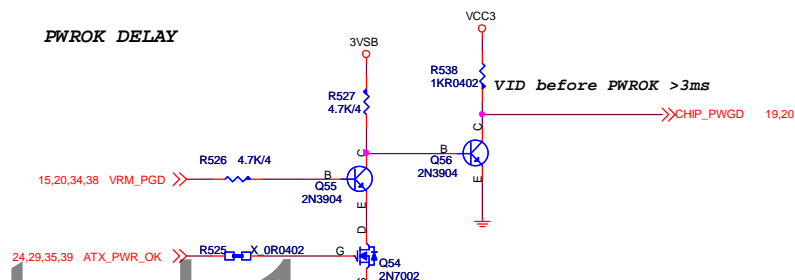
VCC1_8REF



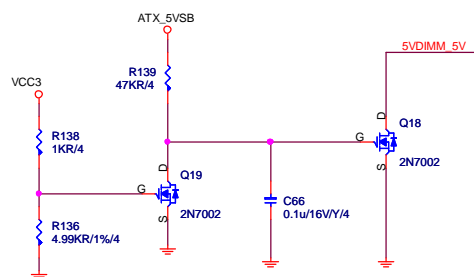
3VSB



PWROK DELAY



Update from SLP_S3# to VRM_PGD



For power 700W solution
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VSDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VSDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



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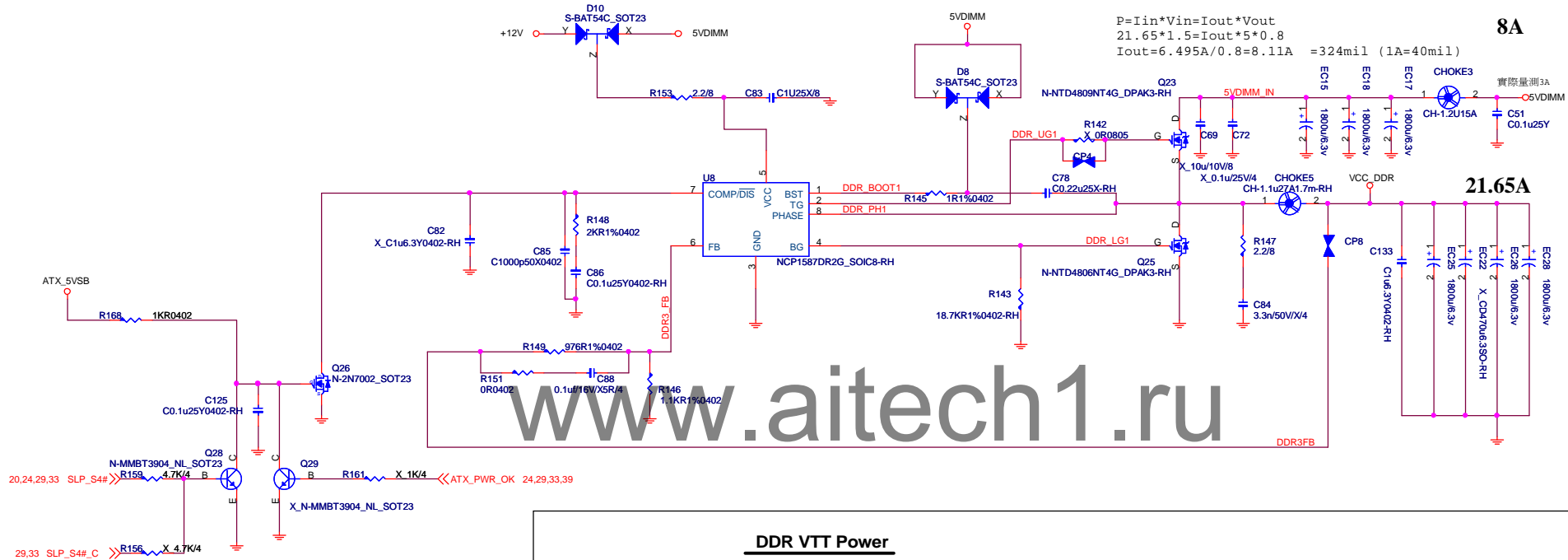
$$\begin{aligned} & \text{DDR_VTT POWER} + \text{CPU(VDDQ)} + \text{VCC} + \text{PCH} \\ &= 3.65 + 2.8 + 7.2 + 8 \\ &= 21.65\text{A} \end{aligned}$$

$$\begin{aligned} I_{\text{ripple}} &= \{ I_o \cdot \sqrt{D} \cdot \sqrt{(1-D)} \} / \text{Phase} \\ &= 21.65 \times 0.547 \times 0.673 \\ &= 7.97\text{A} \\ \text{**Cap} &= 2350\text{m} \times 4 = 9.4\text{A} \end{aligned}$$

DDR3_1.5V

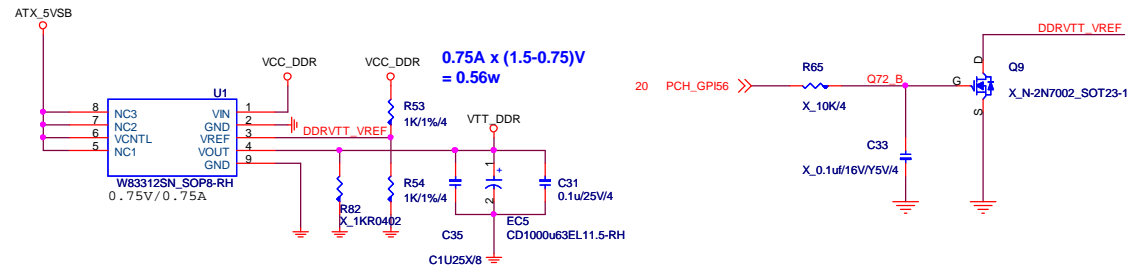
8A

$$\begin{aligned} P &= I_{\text{in}} \cdot V_{\text{in}} = I_{\text{out}} \cdot V_{\text{out}} \\ 21.65 \times 1.5 &= I_{\text{out}} \times 5 \times 0.8 \\ I_{\text{out}} &= 6.495\text{A} / 0.8 = 8.11\text{A} = 324\text{mil} \quad (1\text{A} = 40\text{mil}) \end{aligned}$$



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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CPU_VTT

Cap: $2350\text{m} \cdot 3 = 7.05 \text{ A}$

N4809A

NIKO

D03-0903B4B-N03

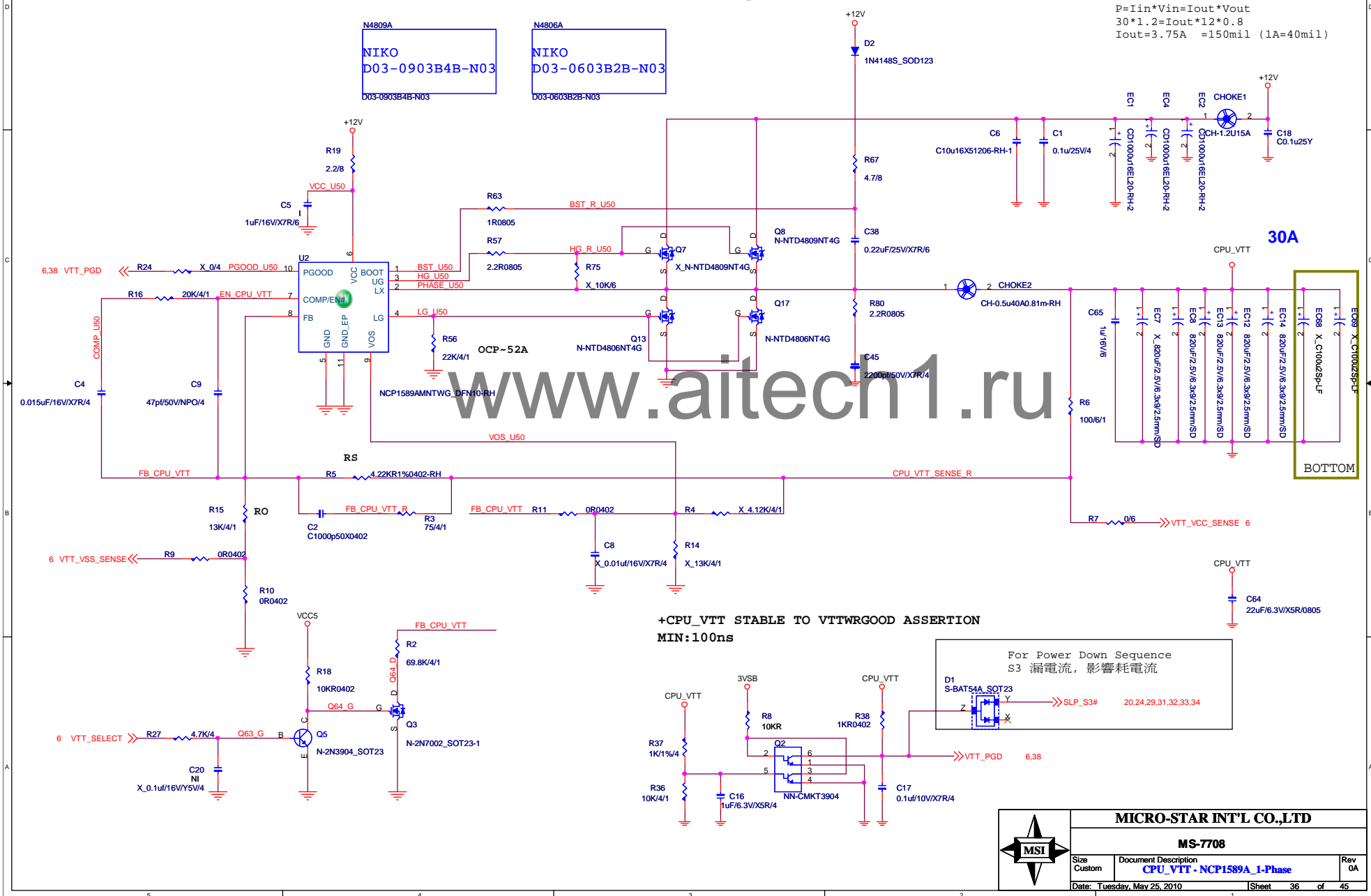
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N4806A

NIKO

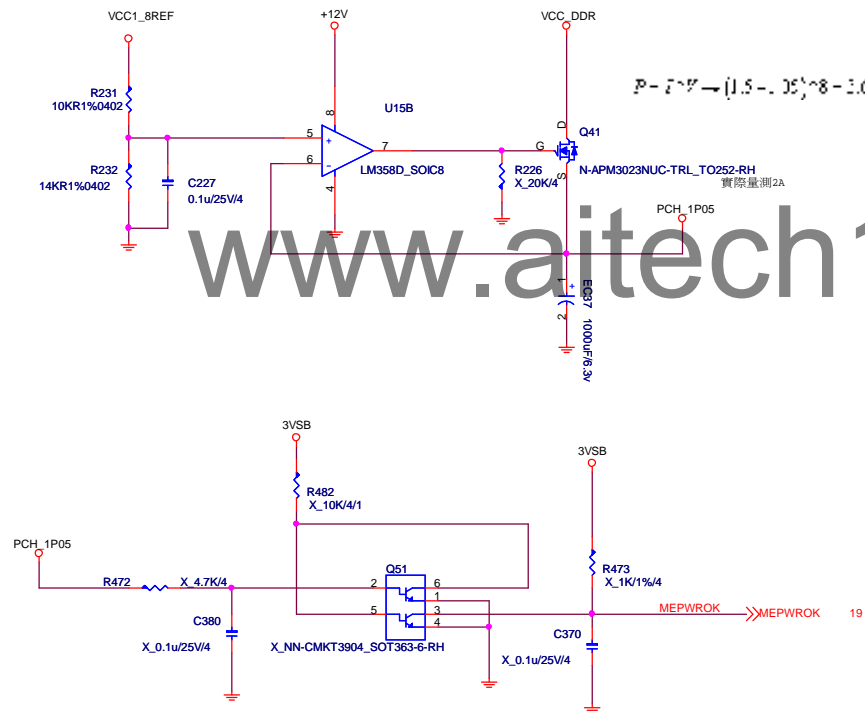
D03-0603B2B-N03

D03-0603B2B-N03



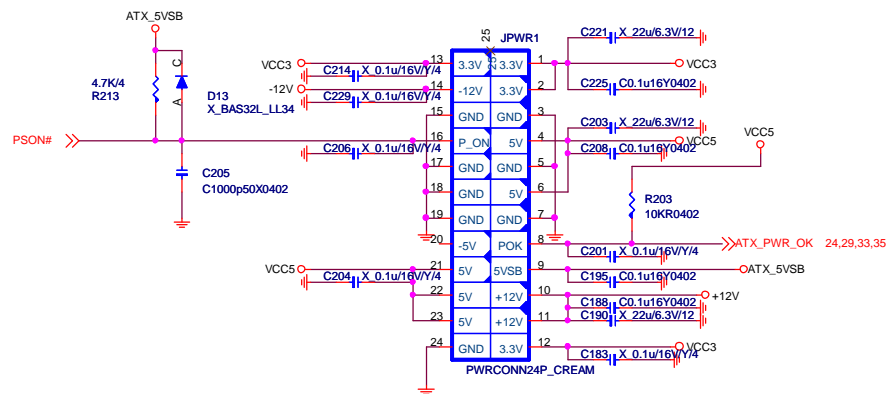
PCH Core

$$5.5\text{A(PCH)} + 2.5\text{A(VCCME)} = 8\text{A}$$

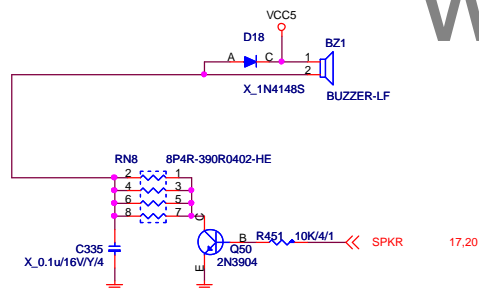
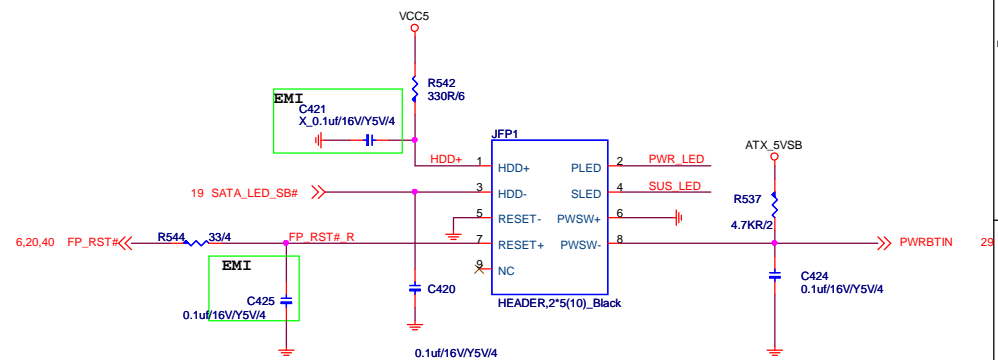


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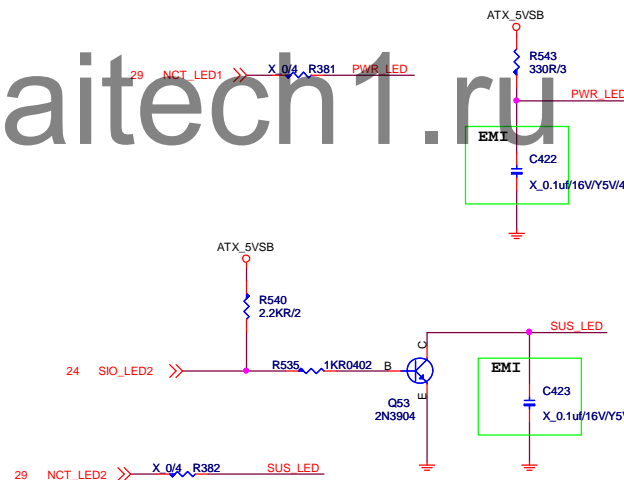
ATX POWER CONNECTOR



FRONT PANNEL



$R=390 \text{ Ohm}$
 $I=(5-0.2)/R=0.123 \text{ A}$
 $W=0.123\text{A} \times 5\text{v}=0.615\text{W}(\text{夠耐電阻})$
 $R=1/16\text{W}=0.062\text{W}$



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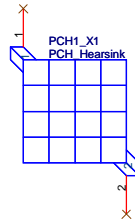
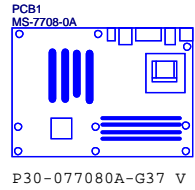
MS-7708

Size Custom Document Description
ATX PWR-Connector/LED

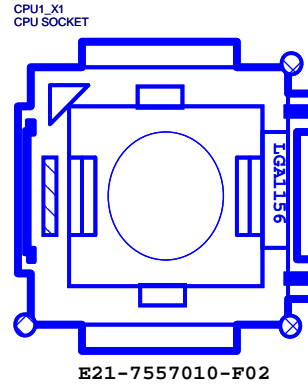
Rev 0A

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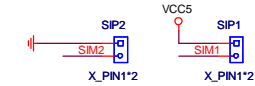
PCB



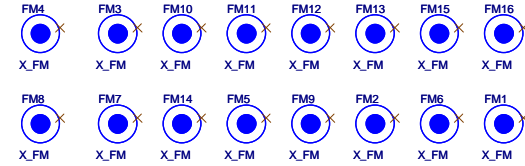
CPU SOCKET



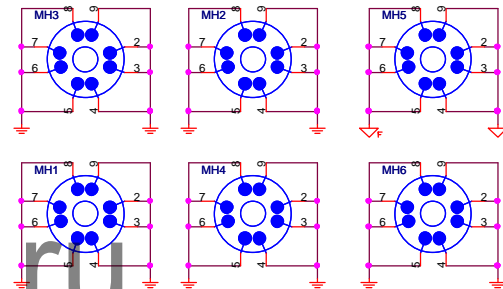
Simulation



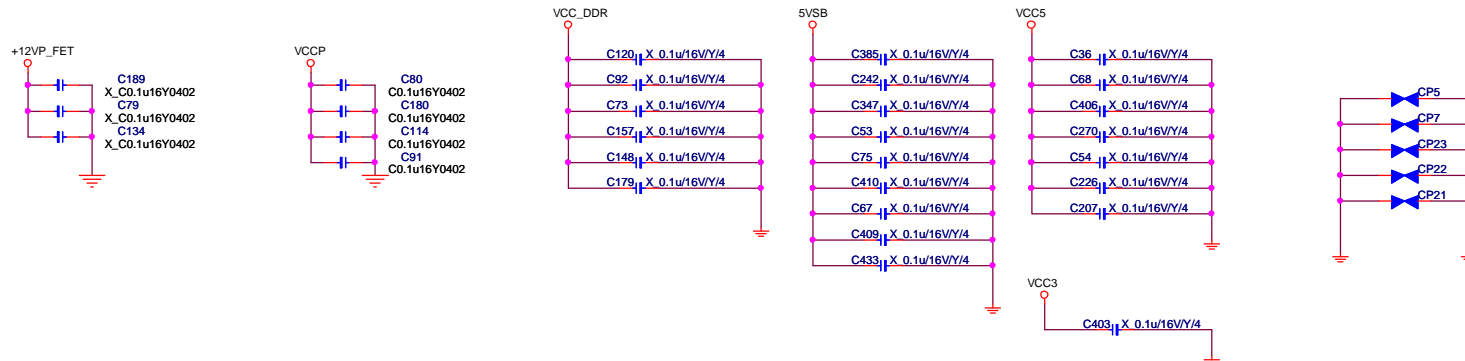
Optical Fiducial Marks-120



Mounting Holes



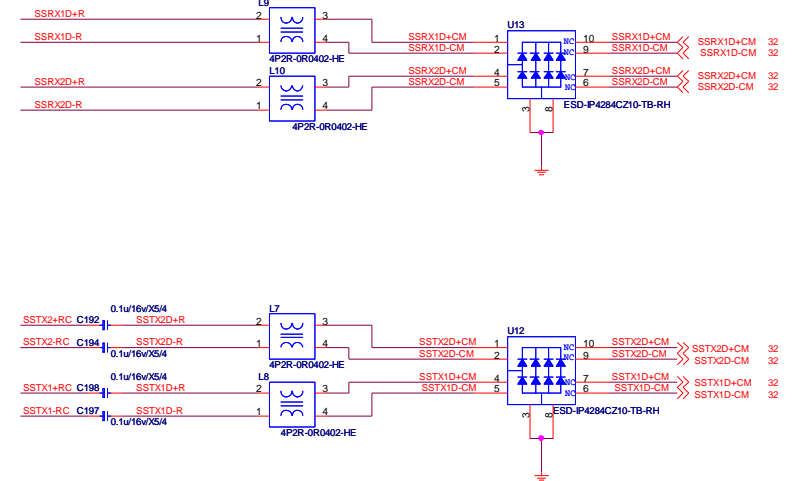
For EMI



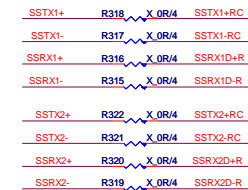
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MS-7708		
Size Custom	Document Description	Rev 0A
Manual & Option parts		
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ESD Protection

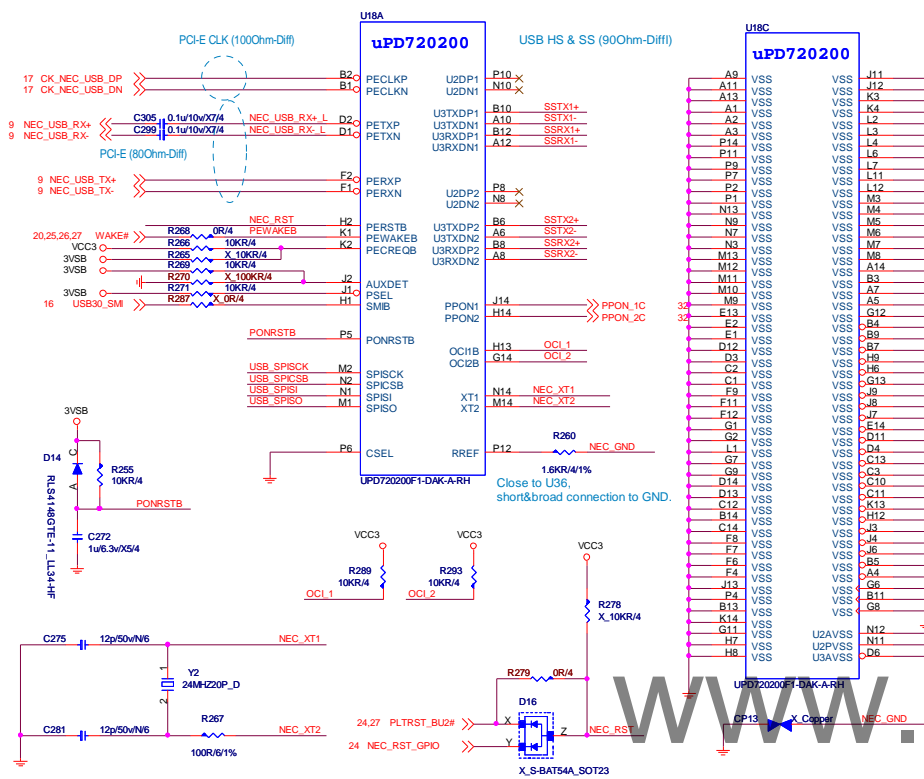
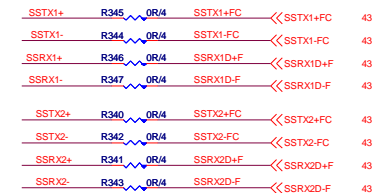
REAR (All component Near the connector)



Stuff for Rear USB3.0



Stuff for Front USB3.0



uPD720200 core Power

NEC_1P05
1.05V
0.7A

AVCC3 STB Power

EEPROM

MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7708			
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Custom	NEC USB3.0		
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20,24,29,31,33,34,36 SLP_S3#

VCC5V 5VSB

C392 $10\mu/10V/Y/R$

900 mA
min 40mil.

U22

S3# OC#

5VCC 5VSB

VOUT VOUT

EN

UP7533A8M8_SOT23-8-RH

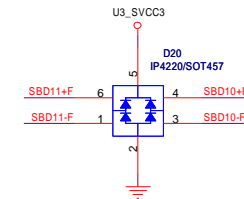
U3_V5VCC3

C364 $0.1\mu/6V/X54$

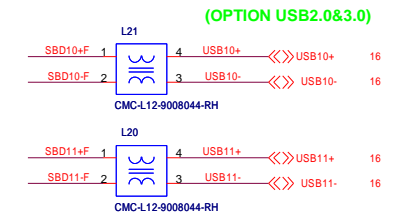
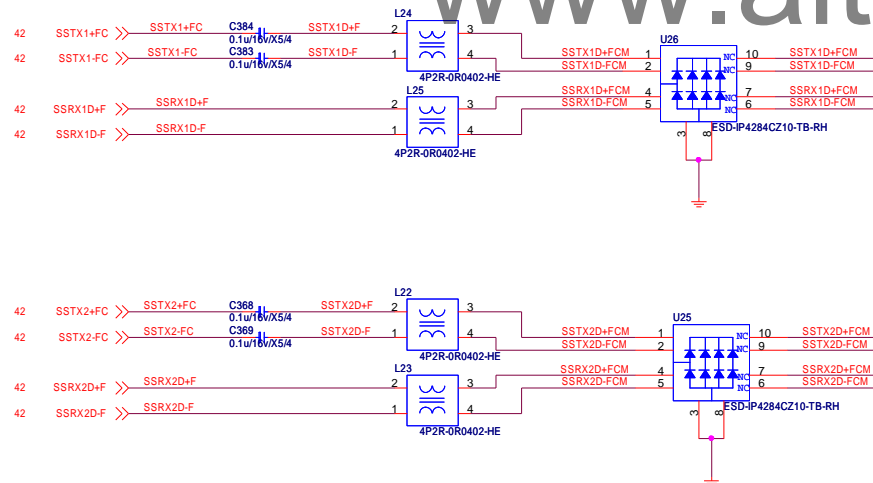
EC56 $470\mu/6V/8\times11.5/3.5mm$


20 PCH_GP44 R499 X_0R/4

42 PPN_2C R498 0R/4



component near the connector)



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	MS-7708		
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